

a buried region of the second conductivity type disposed on said semiconductor substrate;

a uniform base region of the second conductivity type disposed on said first buried region and having a uniform doping profile;

*Sub  
21  
amd.* a plug region of the second conductivity type disposed in said uniform base region, the plug region protrudes from a top surface of said uniform base region so as to reach to said buried region;

*11  
amd.* first and second main electrode regions of the first conductivity type disposed in and at the top surface of said uniform base region, the first and second main electrode regions being aligned in a lateral direction parallel to the top surface of said uniform base region; and

a graded base region of the second conductivity type disposed in said uniform base region, enclosing bottom and side of said first main electrode region such that said first main electrode region is disposed in the center at the top surface of the graded base region, the graded base region having a doping profile such that impurity concentration decreases gradually along the lateral direction towards said second main electrode region from said first main electrode region,

wherein a combination of said uniform base region and said graded base region serves as a base region.

2. (Amended) The lateral transistor of claim 1, wherein said second main electrode region is formed in a ring shape along the top surface of said uniform base region, configured such that said second main electrode region laterally surrounds said graded base region.

*12* 5. (Amended) The lateral transistor of claim 2, further comprising a base wiring being in contact with said base contact region.

6. (Amended) A semiconductor integrated circuit including a lateral transistor, the lateral transistor comprising:

a semiconductor substrate of the first conductivity type;

a first buried region of the second conductivity type disposed on said semiconductor substrate;

a uniform base region of the second conductivity type disposed on said first buried region having a uniform doping profile;

a first plug region of the second conductivity type disposed in said uniform base region, the first plug region protrudes from a top surface of said uniform base region so as to reach to said first buried region;

first and second main electrode regions of the first conductivity type disposed in and at the top surface of said uniform base region, the first and second main electrode regions being aligned in a lateral direction parallel to the top surface of said uniform base region; and

a graded base region of the second conductivity type disposed in said uniform base region, enclosing bottom and side of said first main electrode region such that said first main electrode region is disposed in the center at the top surface of the graded base region, the graded base region has a doping profile such that impurity concentration decreases gradually along the lateral direction towards said second main electrode region from said first main electrode region,

wherein a combination of said uniform base region and said graded base region serves as a first base region of said lateral transistor.

8. (Amended) The semiconductor integrated circuit of claim 7, further comprising a connecting wiring configured to connect said second main electrode region and second base region.

10. (Amended) The lateral transistor of claim 7, wherein said second main electrode region is formed in a ring shape along the top surface of said uniform base

Application No. 10/014,949

First Response

*SUB  
B3  
CMA*  
*14  
CMA* region, configured such that said second ~~main~~ *10* electrode region laterally surrounds said graded base region.

*15* 13. (Amended) The lateral transistor of claim 12, further comprising a first base wiring being in contact with said first base contact region.